REMARKS

The May 25, 2005 Office Action was base on pending Claims 1-11 and Claims 13-21. Thus, after entry of the Amendment, Claims 1-11, and 13-21 are pending and presented for further consideration.

In the May 25, 2005 Office Action, the Examiner rejected Claims 1, 3-5, 7, 8, 10, 11, and 13-21 under 35 U.S.C. § 102(b/e) as being anticipated by U.S. Patent No. 5,303,192 ("the Baba patent") or U.S. Patent No. 6,011,710 ("the Wiggers patent"). The Examiner further rejected Claims 2, 6, and 9 under 35 U.S.C. § 103(a) as being unpatentable over the Baba patent or the Wiggers patent.

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Submitted concurrently herewith is a Supplemental Information Disclosure Statement and form PTO/SB/08 equivalent citing one new reference, which recently came to Applicant's attention in a related application. While the Applicant does not believe that these references will affect the patentability of the pending claims, Applicant respectfully requests the Examiner to consider the pending claims in connection with these references in order to make them of record.

REJECTION OF CLAIMS 1, 3-5, 7, 8, 10, 11 AND 13-21 UNDER 35 U.S.C. § 102(b)

The Examiner rejected Claims 1, 3-5, 7, 8, 10, 11, and 13-21 under 35 U.S.C. § 102(b) as being anticipated by the Baba patent. In view of the following discussion, Applicant respectfully traverses this rejection.

Claims 1, 5, 11

Baba appears to teach a bus line switching circuit selectively connecting N memory elements among M memory elements to N external bus lines. A control circuit appears to detect when the address signal has address information indicative of a defective memory cell and to control the bus switch so that memory elements having defective blocks are not selected.

Baba **does not** teach interfacing a state controller with a memory controller. Baba does **not teach** controlling the bus switch to reduce data bus capacitance. The

bus line switching circuit 20 **is not** a state controller and the controller 24 **is not** a memory controller. The controller 24 compares the ADD signal with the contents of the ROM 24a to determine if the address is accessing defective blocks of memory. The controller 24 controls the bus line switching circuit 20 so that it selects a memory chip having no defective memory block. See figure 3 and column 6 lines 21-34.

In contrast, in an embodiment of the invention, a method of making a memory module comprises interfacing a state decoder with a memory controller, where the state decoder selectively controls a bus switch to reduce data bus capacitance.

The reference cited by the Examiner does not disclose, teach, or suggest the use of a state decoder and a memory controller where the state decoder selectively controls a bus switch to reduce data bus capacitance. Applicant asserts that Claims 1, 5, and 11 are not anticipated by the Baba patent. Applicant therefore respectfully submits that Claims 1, 5, and 11 are patentably distinguished over the cited reference and Applicant respectfully requests allowance of Claims 1, 5, and 11.

Claims 3, 4, 7, 8, 10, and 13-21

Claims 3, 4, and 13-16, which depend from Claim 1, and Claims 7, 8, 10, and 17, which depend from Claim 5, and Claims 18-21, which depend from Claim 11, are believed to be patentable for the same reasons articulated above with respect to Claims 1, 5 and 11, respectively, and because of the additional features recited therein.

REJECTION OF CLAIMS 1, 3-5, 7, 8, 10, 11, and 13-21 UNDER 35 U.S.C. § 102(e)

The Examiner rejected Claims 1, 3-5, 7, 8, 10, 11, and 13-21 under 35 U.S.C. § 102(e) as being anticipated by the Wiggers patent. In view of the following discussion, Applicant respectfully traverses this rejection.

Claims 1, 5, 11

Wiggers also does not appear to teach interfacing a state controller with a memory controller, where the state decoder controls the bus switch to reduce data bus capacitance.

Wiggers appears to teach controlling the switches with a signal from the memory controller. See column 5, lines 40-47. The memory controller 21 produces the control signal 31 and the terminal 37 of the switch 29A receives the control signal 31 to control the switching of the terminals 35, 36 of the switch 29A. The memory controller 21 **is not** a state controller and the main board 25 **is not** a memory controller. Wiggers **does not** teach a state controller **and** a memory controller. See figures 3 and 4.

In contrast, in an embodiment of the invention, a method of making a memory module comprises interfacing a state decoder with a memory controller, where the state decoder selectively controls a bus switch to reduce data bus capacitance.

The reference cited by the Examiner does not disclose, teach, or suggest the use of a state decoder and a memory controller where the state decoder selectively controls a bus switch to reduce data bus capacitance. Applicant asserts that Claims 1, 5, and 11 are not anticipated by the Wiggers patent. Applicant therefore respectfully submits that Claims 1, 5, and 11 are patentably distinguished over the cited reference and Applicant respectfully requests allowance of Claims 1, 5, and 11.

Claims 3, 4, 7, 8, 10, and 13-21

Claims 3, 4, and 13-16, which depend from Claim 1, and Claims 7, 8, 10, and 17, which depend from Claim 5, and Claims 18-21, which depend from Claim 11, are believed to be patentable for the same reasons articulated above with respect to Claims 1, 5 and 11, respectively, and because of the additional features recited therein.

REJECTION OF CLAIMS 2, 6, AND 9 UNDER 35 U.S.C. § 103(a)

The Examiner rejected Claims 2, 6, and 9 under 35 U.S.C. § 103(a) as being unpatentable over the Baba patent or the Wiggers patent.

Claim 2, which depends from Claim 1, and Claims 6 and 9, which depend from Claim 5, are believed to be patentable for the same reasons articulated above with respect to Claims 1 and 5, respectively, and because of the additional features recited therein.

REQUEST FOR TELEPHONE INTERVIEW

Pursuant to M.P.E.P. § 713.01, in order to expedite prosecution of this application, Applicant's undersigned attorney of record hereby formally requests a telephone interview with the Examiner as soon as the Examiner has considered the effect of the arguments presented above. Applicant's attorney can be reached at (949) 721-2998 or at the number listed below.

CONCLUSION

Applicant has endeavored to address all of the Examiner's concerns as expressed in the outstanding Office Action. In light of the above remarks, reconsideration and withdrawal of the outstanding rejections is specifically requested.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 7/18/05

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